AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) An oversampling clock recovery method comprising the steps of: generating non-uniform multi-phase clock signals having a non-uniform interval, said non-uniform multi-phase clock signals comprising three or more phase clock signals for one bit of an input data; controlling a phase of said non-uniform multi-phase clock signals so that a phase of one of two edges in two-phase clock signals having a relative narrower interval among said non-uniform multi-phase clock signals is locked with a phase of a transition point of said input data; digitally controlling, by using selection circuits and delay locked loops each comprising a plurality of delay buffers, phases of two or more sets of uniform multi-phase clock signals having a uniform interval at a resolution less than a propagation delay of a delay buffer in said delay locked loops; keeping, by said digital control, a phase difference between a set of uniform multi-phase clock signals and another set of uniform multi-phase clock signals to a phase difference shorter than said propagation delay; and using a combination of said two or more sets of uniform multi-phase clock signals as said non-uniform multi-phase clock signals.

2. (Original) An oversampling clock recovery method as claimed in claim 1, wherein said non-uniform multi-phase clock signals ~~comprises~~ comprise three-phase clock signals for one bit of said input data.

11. (Original) An oversampling clock recovery method comprising the steps of: generating non-uniform multi-phase clock signals having a non-uniform interval, said non-uniform multi-phase clock signals comprising four or more phase clock signals for one bit of an input data; controlling a phase of said non-uniform multi-phase clock signals so that a phase of one of two clock edges in a first set of clock signals having a relative narrower interval among said non-uniform multi-phase clock signals is phase locked with a phase of a transition point of said input data; and controlling a phase of said non-uniform multi-phase clock signals so as to avoid making a phase of one of two clock edges in a second set of clock signals having a relative narrower interval among said non-uniform multi-phase clock signals phase lock with the phase of the transition point of said input data, said second set of clock signals being apart from said first set of clock signals through a relatively wider phase interval by about a length of half bit of said input data.

12. (Currently amended) An oversampling clock recovery method as claimed in claim 11, wherein said non-uniform multi-phase clock signals ~~comprises~~ comprise four-phase clock signals for one bit for said input data.

13. (Currently amended) An oversampling clock recovery method as claimed in claim 11, wherein said method further comprises the steps of: digitally controlling, by using selection circuits and delay locked loops each comprising a plurality of delay buffers, phases of two or more sets of uniform multi-phase clock signals having uniform interval at a resolution shorter than a propagation delay of a delay buffer in said delay locked loops; keeping, by said digital control, a phase difference between a set of uniform multi-phase clock signals and another set of uniform multi-phase clock signals to a phase difference shorter than said propagation delay; and using a combination of said two or more sets of uniform multi-phase clock signals as said non-uniform multi-phase clock signals.

14. (Currently amended) An oversampling clock recovery method as claimed in claim 11, wherein said step of controlling the phase of said non-uniform multi-phase clock signals is carried out by using a digital phase control method which comprises the steps of: preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval; preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval; phase locking a specific clock signal in said first multi-phase clock signals and a particular clock signal in said second multi-phase clock signals; and changing a combination of the specific and the particular clock signals to be phase-locked to shift a phase of said second multi-phase clock signals.

15. (Currently amended) An oversampling clock recovery method as claimed in claim 11, wherein said step of controlling the phase of said non-uniform multi-phase clock signals is carried out by a digital phase control method which comprises the steps of: preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval; preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval; preparing third multi-phase clock signals having the second uniform phase interval; phase locking a specific clock signal in said first multi-phase clock signals and a first particular clock signal in said second multi-phase clock signals; phase locking ~~[a]~~ said specific clock signal in said first multi-phase clock signals and a second particular clock signal in said third multi-phase clock signals; and changing a combination of the specific clock signal and the first particular clock signal to be phase-locked and a combination of the specific clock signal and the second particular clock signal to be phase-locked, thereby controlling phases of said second and said third multi-phase clock signals for use in sampling said input data with a phase difference between said second multi-phase clock signals and said third multi-phase clock signals kept.

16. (Original) An oversampling clock recovery method as claimed in claim 15, wherein the resolution for controlling the phases of said second and said third multi-phase clock signals is equal to the phase difference between said second multi-phase clock signals and said third multi-phase clock signals.